| Ref # | Hits | Search Query | DBs | Default Operator | Plurals | Time Stamp |
|---|---|---|---|---|---|---|
| L1 | 7947 | via and trench and (amorphous or crystalline or polycrystalline) | US-PGPUB; USPAT | OR | ON | 2005/02/08 10:49 |
| L2 | 7297 | 1 and @ad<"20030923" | US-PGPUB; USPAT | OR | ON | 2005/02/08 10:49 |
| L3 | 4077 | 2 and (second with (dielectric or insulative or insulating or insulator)) | US-PGPUB; USPAT | OR | ON | 2005/02/08 10:05 |
| L4 | 3327 | 3 and oxide and nitride | US-PGPUB; USPAT | OR | ON | 2005/02/08 10:06 |
| L5 | 2783 | 3 and oxide and (silicon adj nitride) | US-PGPUB; USPAT | OR | ON | 2005/02/08 10:06 |
| L6 | 2602 | 3 and (silicon adj (oxide or dioxide)) and (silicon adj nitride) | US-PGPUB; USPAT | OR | ON | 2005/02/08 10:07 |
| L7 | 1033 | 6 and (annealing or crystallizing) | US-PGPUB; USPAT | OR | ON | 2005/02/08 10:59 |
| L8 | 395 | 7 and (planarizing or planarization) | US-PGPUB; USPAT | OR | ON | 2005/02/08 10:50 |
| L9 | 89 | via and trench and (amorphous or crystalline or polycrystalline) | USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2005/02/08 10:57 |
| L10 | 107 | via with trench with (amorphous or crystalline or polycrystalline) | US-PGPUB; USPAT | OR | ON | 2005/02/08 10:49 |
| L11 | 100 | 10 and @ad<"20030923" | US-PGPUB; USPAT | OR | ON | 2005/02/08 10:59 |
| L12 | 83 | 11 not 8 | US-PGPUB; USPAT | OR | ON | 2005/02/08 10:50 |
| L15 | 1100 | via with trench with silicon | US-PGPUB; USPAT | OR | ON | 2005/02/08 11:17 |
| L16 | 1029 | 15 and @ad<"20030923" | US-PGPUB; USPAT | OR | ON | 2005/02/08 11:18 |
| L17 | 263 | 16 and (annealing or crystallizing) | US-PGPUB; USPAT | OR | ON | 2005/02/08 11:00 |
| L18 | 282 | via with trench with channel | US-PGPUB; USPAT | OR | ON | 2005/02/08 11:31 |
| L19 | 259 | 18 and @ad<"20030923" | US-PGPUB; USPAT | OR | ON | 2005/02/08 11:31 |
| L20 | 93 | 19 and (silicon with channel) | US-PGPUB; USPAT | OR | ON | 2005/02/08 11:18 |
| L21 | 142 | via same trench same (trench adj gate) | US-PGPUB; USPAT | OR | ON | 2005/02/08 11:37 |
| L22 | 124 | 21 and @ad<"20030923" | US-PGPUB; USPAT | OR | ON | 2005/02/08 11:43 |

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|---|---|---|---|---|---|---|
| L23 | 117 | 22 and silicon | US-PGPUB; USPAT | OR | ON | 2005/02/08 11:31 |
| L24 | 79 | 23 not 19 | US-PGPUB; USPAT | OR | ON | 2005/02/08 11:31 |
| L25 | 31 | via same trench same (trench adj gate) | USOCR; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2005/02/08 11:37 |
| L26 | 115 | (trench adj pad) and @ad<"20030923" | US-PGPUB; USPAT | OR | ON | 2005/02/08 11:49 |
| L27 | 3872 | (trench same via same (semiconductor or SiGe or GaAs or InSb)) and @ad<"20030923" | US-PGPUB; USPAT | OR | ON | 2005/02/08 11:50 |
| L28 | 1601 | (trench with via with (semiconductor or SiGe or GaAs or InSb)) and @ad<"20030923" | US-PGPUB; USPAT | OR | ON | 2005/02/08 11:50 |
| L29 | 128 | (trench with via with (Si or SiGe or GaAs or InSb)) and @ad<"20030923" | US-PGPUB; USPAT | OR | ON | 2005/02/08 12:46 |
| L30 | 1762 | (trench with (Si or SiGe or GaAs or InSb)) and @ad<"20030923" | US-PGPUB; USPAT | OR | ON | 2005/02/08 12:46 |
| L31 | 1634 | 30 not 29 | US-PGPUB; USPAT | OR | ON | 2005/02/08 12:46 |
| L32 | 1603 | 31 not 8 | US-PGPUB; USPAT | OR | ON | 2005/02/08 12:46 |
| L33 | 1599 | 32 not 11 | US-PGPUB; USPAT | OR | ON | 2005/02/08 12:47 |
| L34 | 1567 | 33 not 16 | US-PGPUB; USPAT | OR | ON | 2005/02/08 12:47 |
| L35 | 1558 | 34 not 19 | US-PGPUB; USPAT | OR | ON | 2005/02/08 12:47 |
| L36 | 1556 | 35 not 22 | US-PGPUB; USPAT | OR | ON | 2005/02/08 12:47 |
| L37 | 1556 | 36 not 24 | US-PGPUB; USPAT | OR | ON | 2005/02/08 12:47 |
| L38 | 1544 | 37 not 26 | US-PGPUB; USPAT | OR | ON | 2005/02/08 12:49 |
| L39 | 1339 | 38 and(dielectric or insulating or insulator or insulative) | US-PGPUB; USPAT | OR | ON | 2005/02/08 12:49 |

US-PAT-NO: 6239465

DOCUMENT-IDENTIFIER: US 6239465 B1

TITLE: Non-volatile semiconductor memory device having vertical transistors with the floating and control gates in a trench and fabrication method therefor

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Detailed Description Text - DETX (8):

As shown in FIG. 4C, an insulating film such as a nitride film (Si.sub.3 N.sub.4 200 nm thick) is grown on the whole surface of the epitaxial layer 25, and a pattern (at positions indicated by 26 in FIG. 3) having narrow windows only on the device separation areas parallel to the word lines (43 in FIG. 3) is formed by a photolithography technology. Silicon (**Si**) is vertically etched with this pattern serving as a mask to form **trenches** 1.5 .mu.m deep in the device separation areas. The bottom of the trenches are deeper than the lower part of the buried n.sup.+ diffusion layer 24 and the trenches completely separate the n.sup.+ diffusion layer 24. The trenches are then filled back with oxide films by a usual method of chemical vapor deposition and etch back processes to form trench-type insulating walls (trench isolation) 26. The source n.sup.+ diffusion layer 24 is separated in a strip manner from each other by the trench-type insulating walls 26. Before the trenches are filled with the oxide films, ion implantation is performed at such an angle from the vertical side wall that p.sup.+ diffusion layers (not shown) for channel cut along the side walls and the bottoms of the trenches are formed, that is, on surfaces of the p-type epitaxial layer 25 and the p-type substrate 21 with which the trench-type insulation 26 is in contact.

Detailed Description Text - DETX (12):

As shown in FIG. 4G, the side-wall insulating film 31 and the insulating film 29 are removed. A tunneling oxide film 33 (SiO.sub.2 10 nm thick) is grown on the entire surface of the exposed silicon (Si), that is, the top surface of the drain region 28, inside walls and bottoms of the first and second 30, 32, respectively, by thermal oxidation. A polycrystalline silicon film 34 (poly-**Si** 100 nm thick) doped with phosphorus, to be used as a floating gate electrode, is deposited on the tunneling oxide film 33, and then strip patterns which cover the upper portions of the second **trenches** 32 and are separated by the device areas in the word-line (WL) direction, are formed by the photolithography technology.